

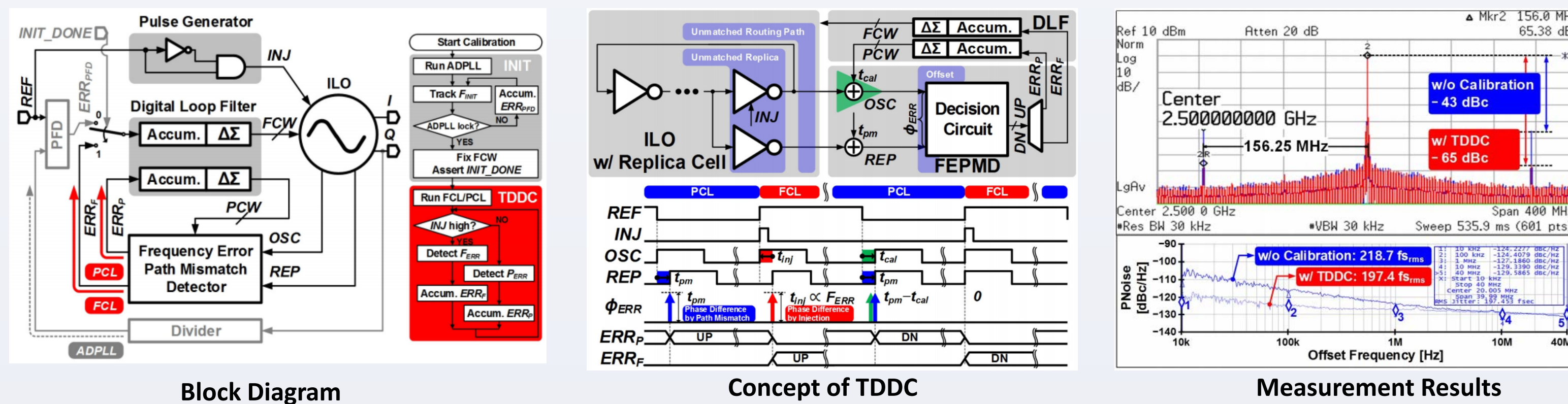
Integrated Systems Design Laboratory

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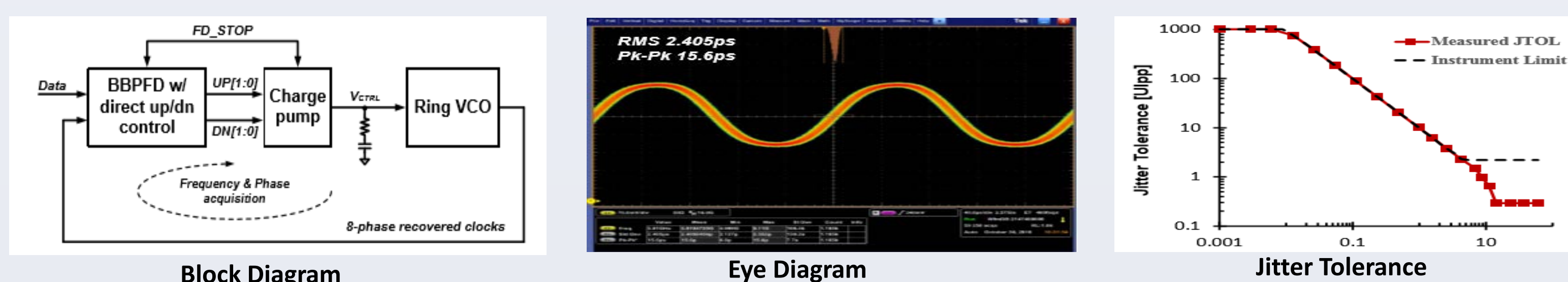
PDCI (PLL, DLL, CDR, ILO)

◆ Injection locked- All Digital Phase Locked Loop



- Low Jitter Injection locked ADPLL
- Reduction of Reference Spur using Time Division Dual Calibration

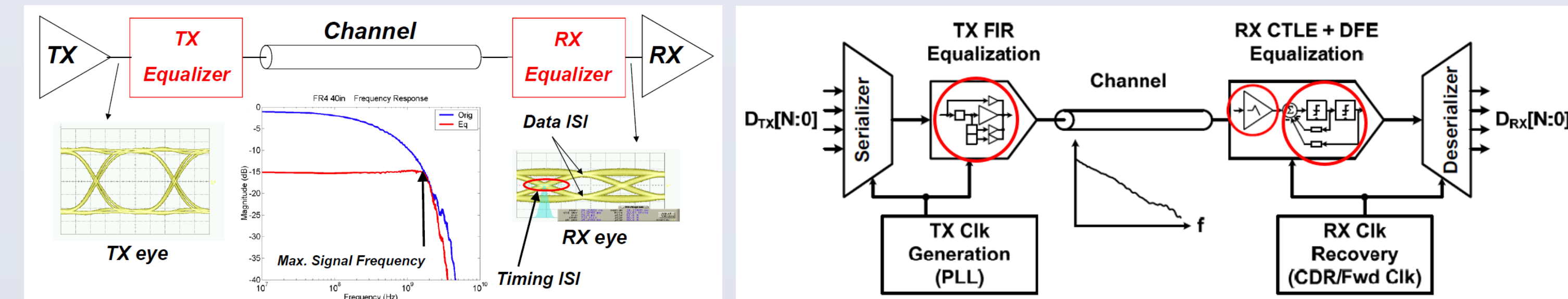
◆ Reference-less Clock and Data Recovery



- Wide range Single loop Reference-less CDR

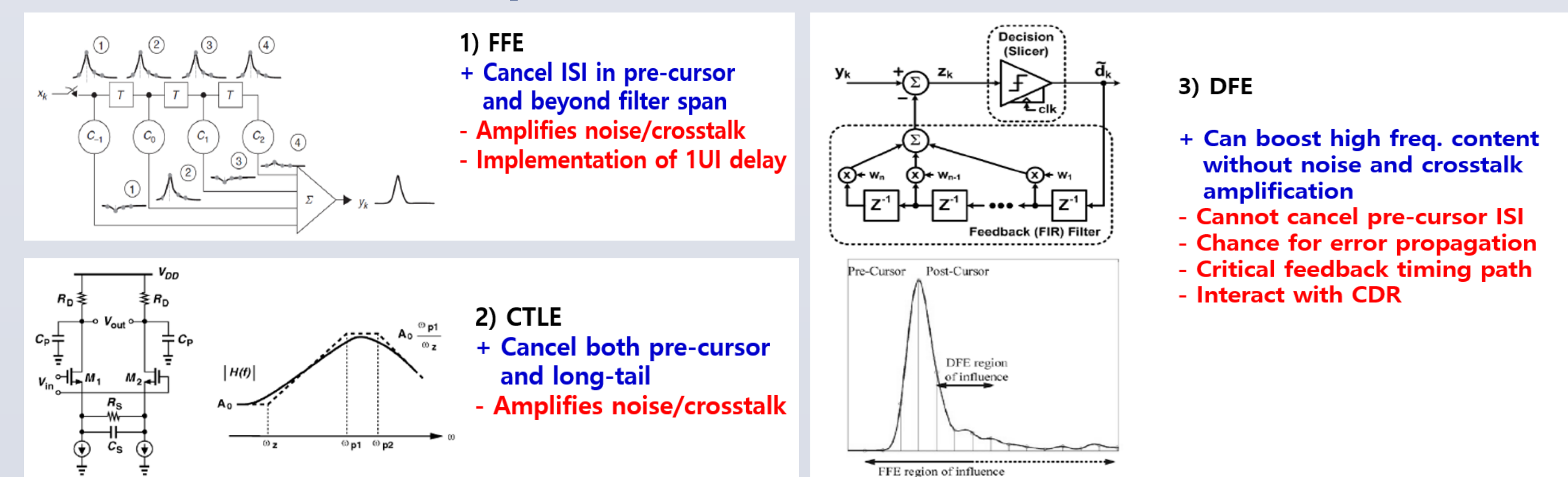
Equalizer

◆ Basic Concept of Equalization



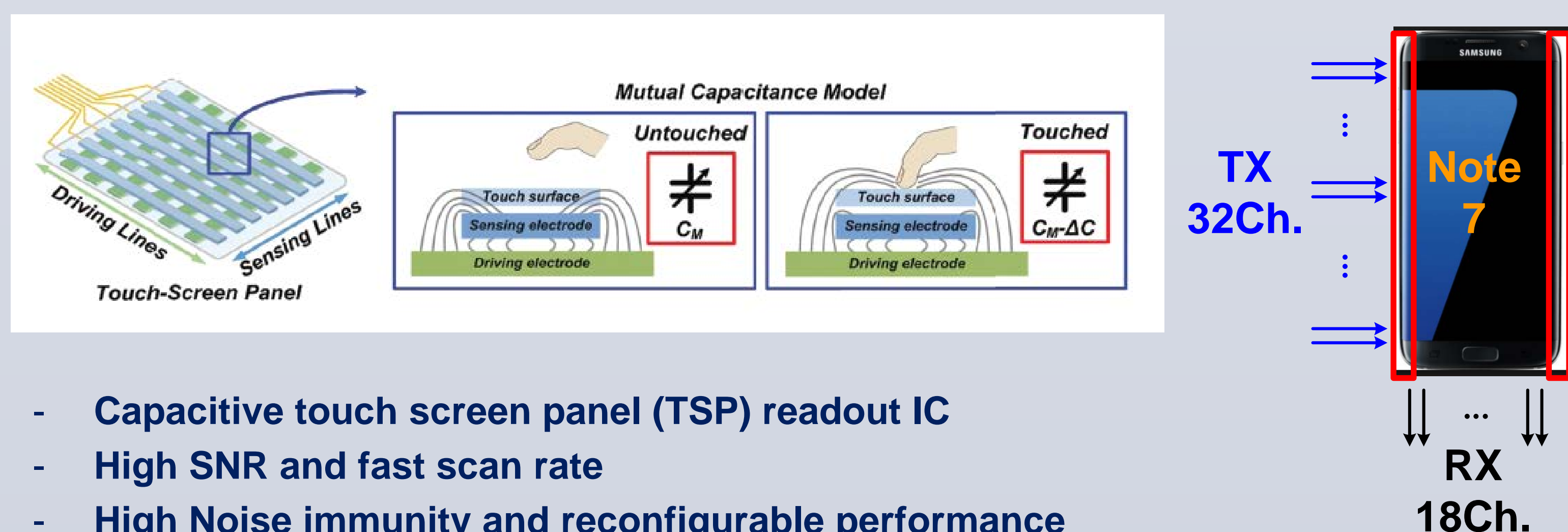
- Compensate the channel loss for high-frequency data transmission
- Tx Equalizer & Rx Equalizer
- Maximum Eye-Opening is desired

◆ Three Kinds of Equalizer and Characteristics

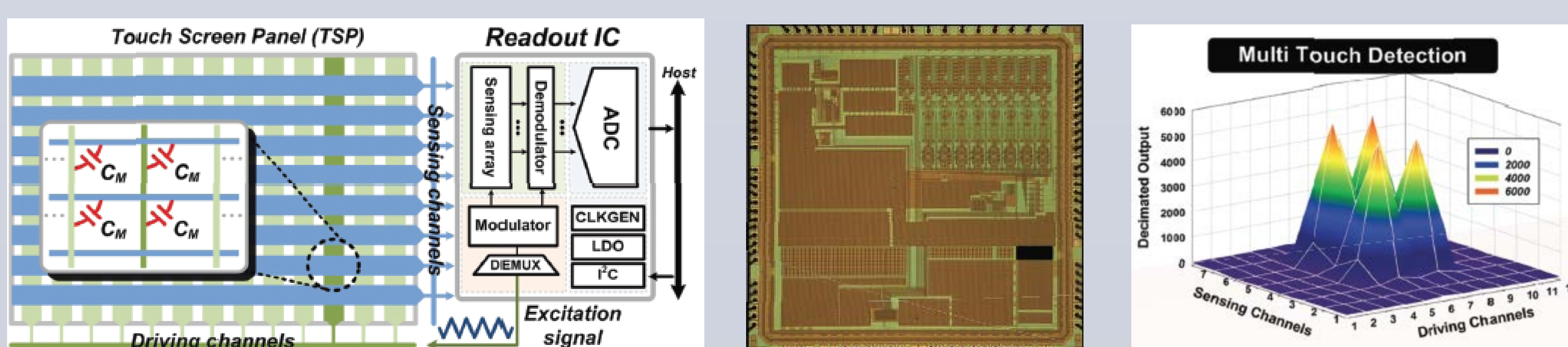


Touch Screen Controller (TSC)

◆ Overall System Architecture and Fundamentals

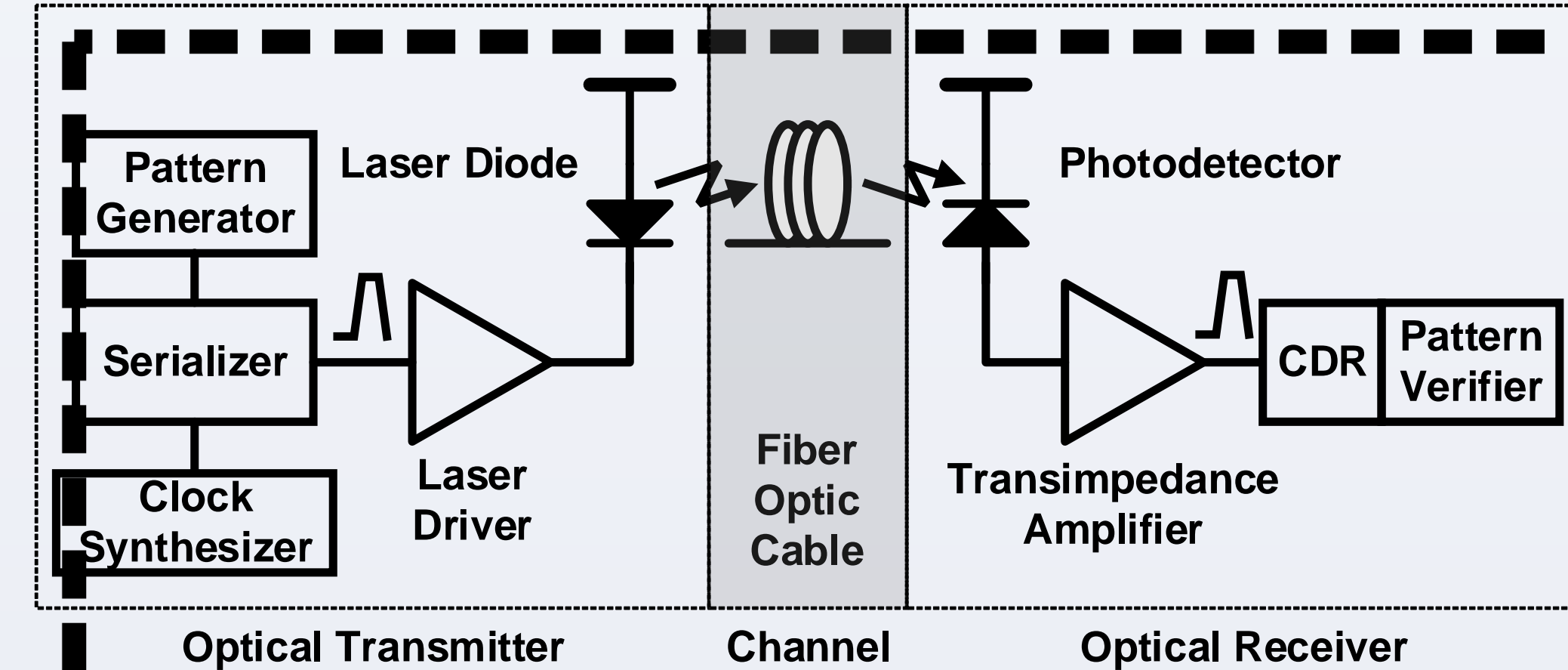


- Capacitive touch screen panel (TSP) readout IC
- High SNR and fast scan rate
- High Noise immunity and reconfigurable performance



Silicon Photonics

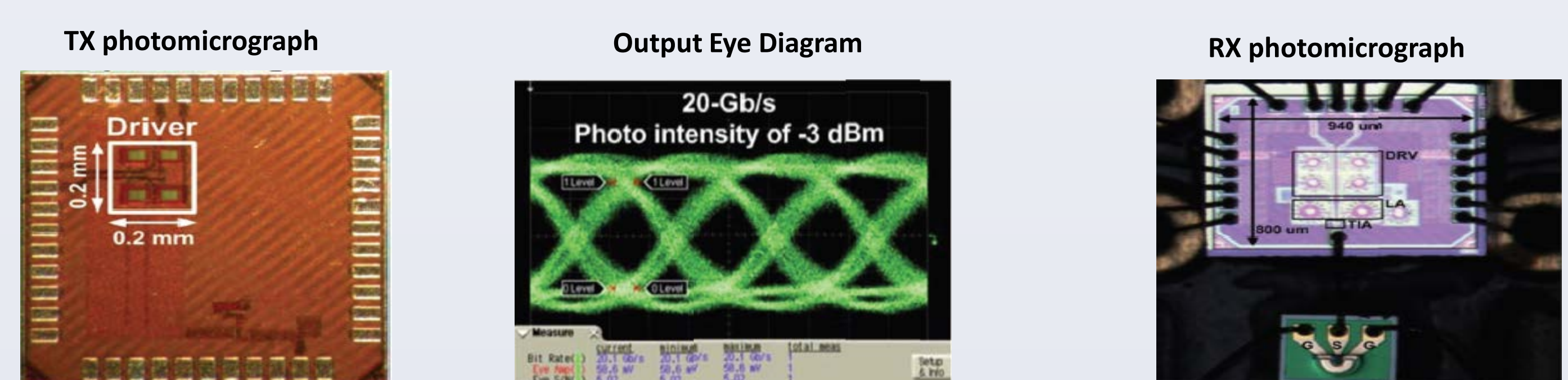
◆ Overall Optical Communication System



Optical Transmitter Channel Optical Receiver

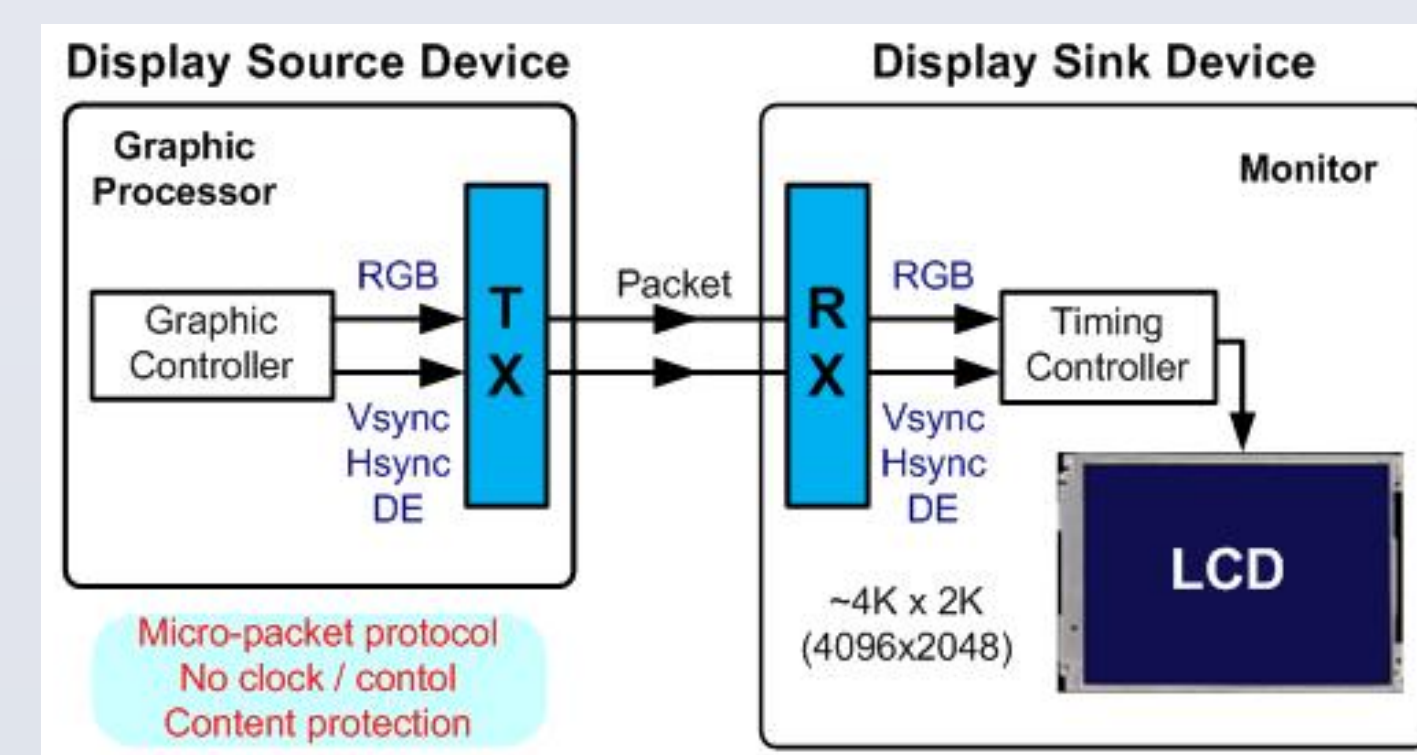
- CMOS interface circuits for silicon photonics
- High-voltage, High bandwidth driver
- Low-power, High – Speed TIA

◆ TRX Chip & Measurement Eye Diagram

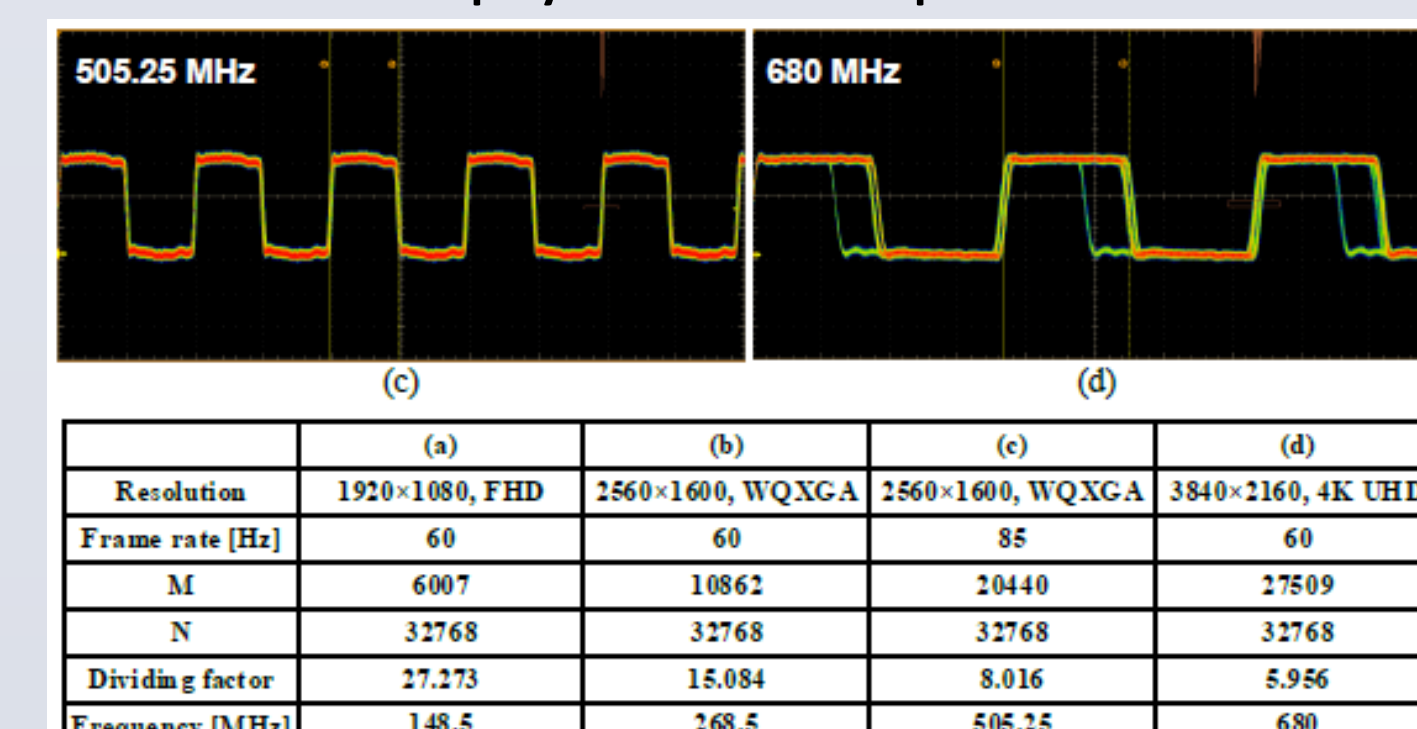


Display Port (DP)

◆ Display Port Interface

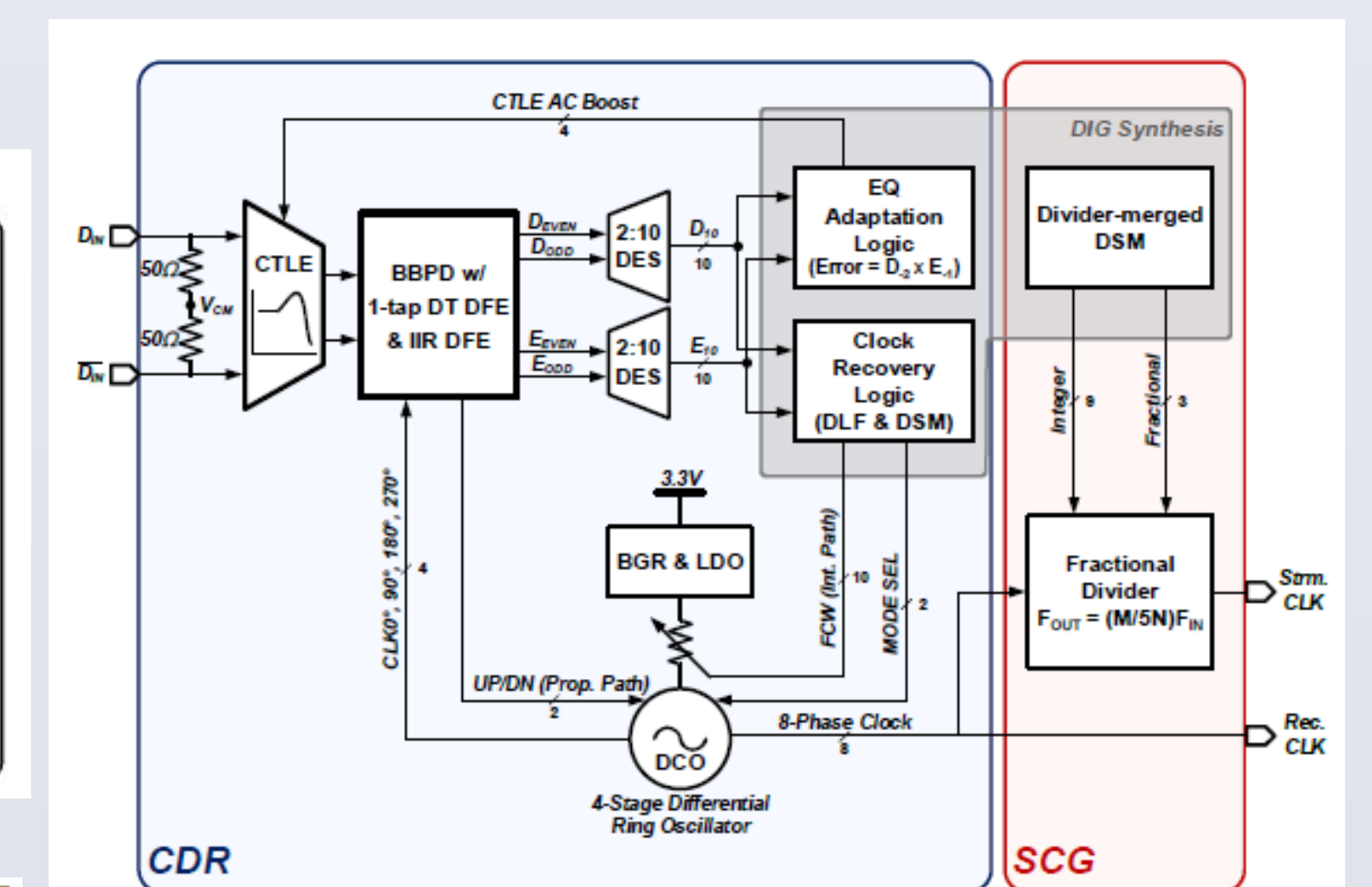


Display Port Data Transport

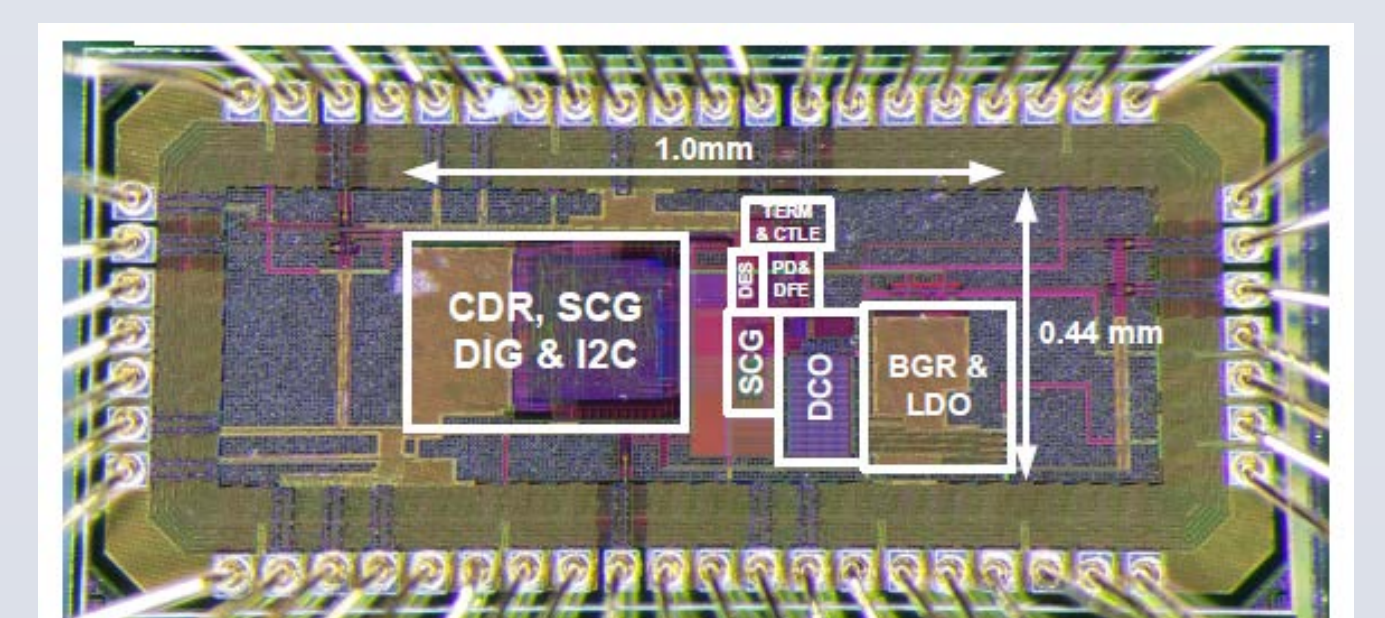


Stream clocks of various display resolutions

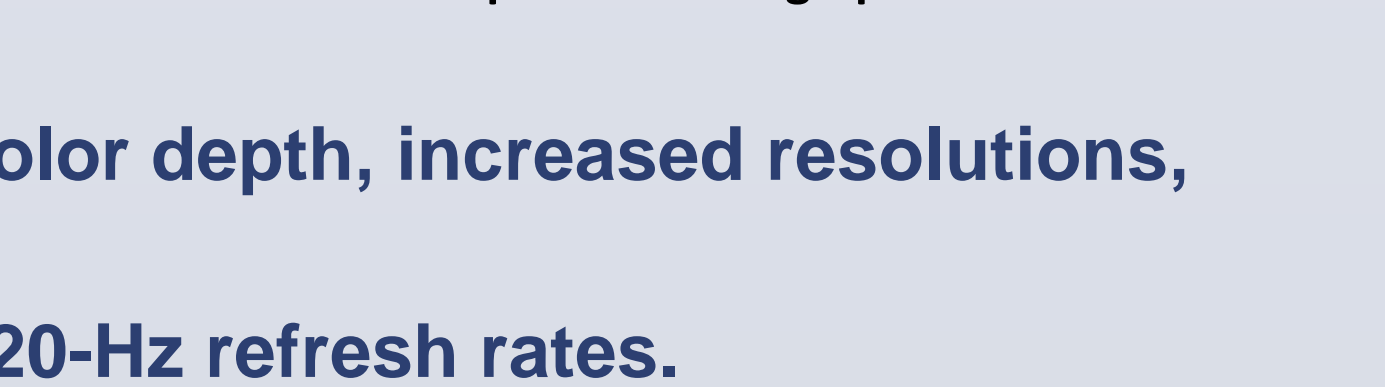
- Display Port supports up to 32.4 Gbps
- Increased display data due to greater color depth, increased resolutions, and higher refresh rates
- Provides quad full HD (3840X2160) at 120-Hz refresh rates.



Receiver Architecture

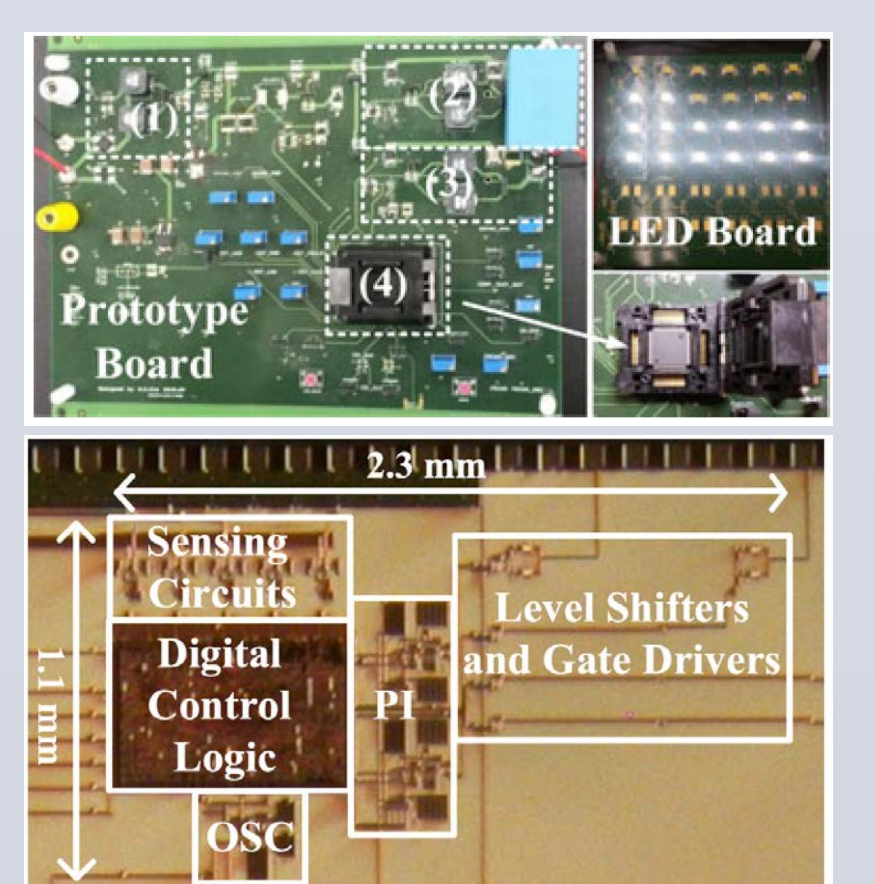
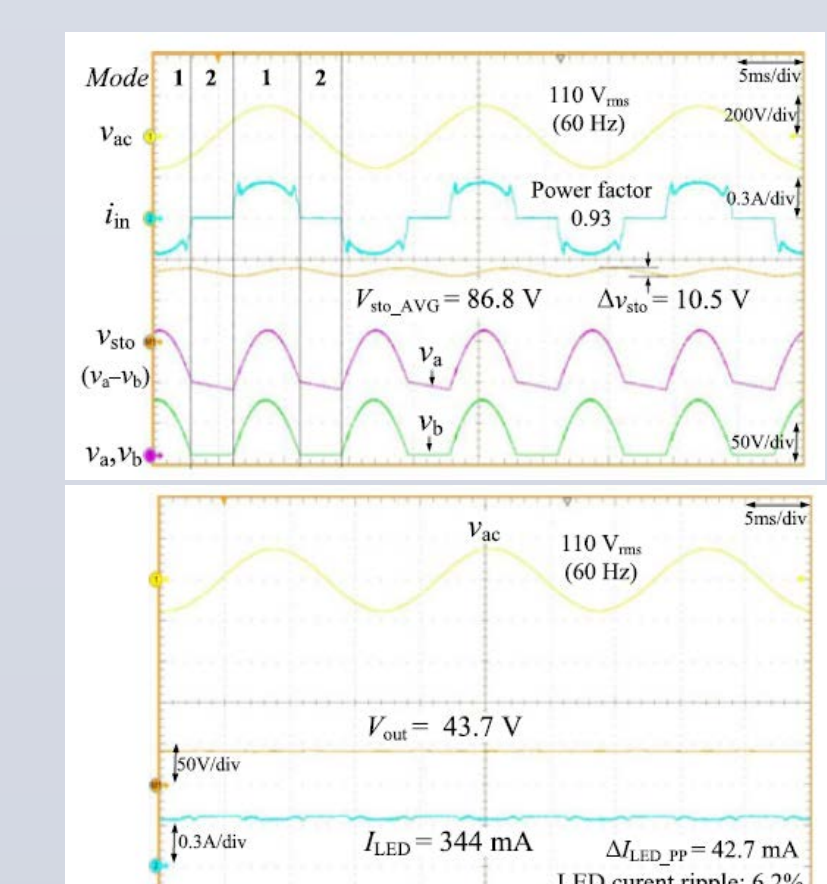
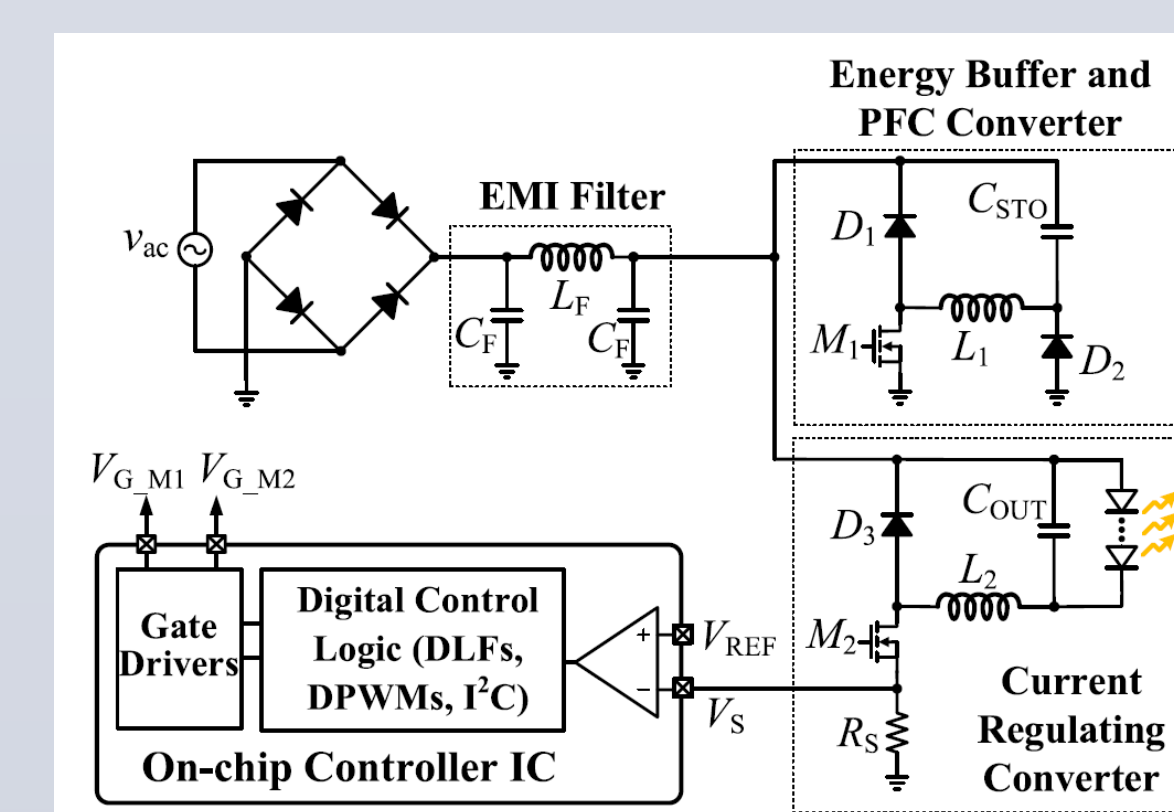


Chip Photomicrograph



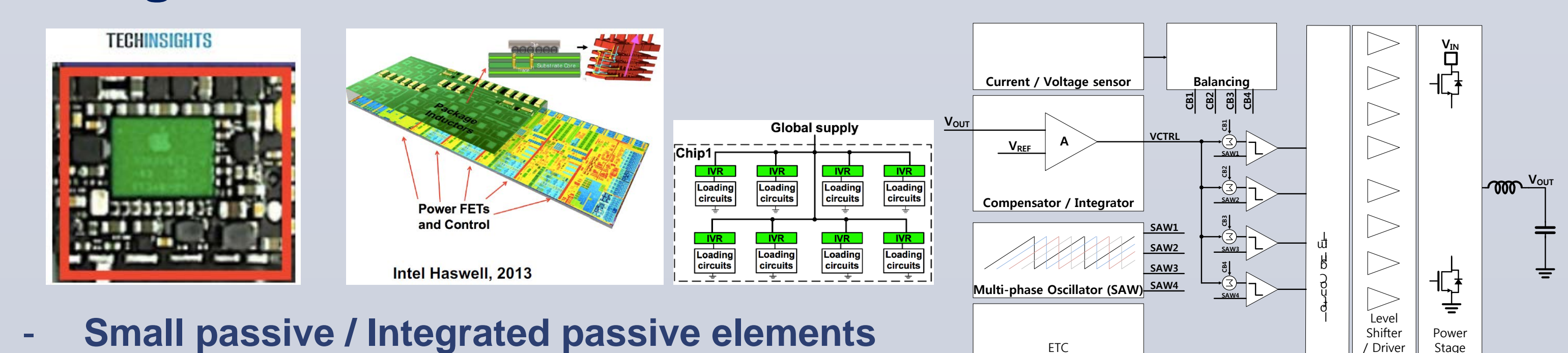
Power Management IC (PMIC)

◆ LED Driver



- AC-DC LED Driver topology and controller IC design

◆ Integrated DC-DC converter desi



- Small passive / Integrated passive elements
- High frequency controller design