VLSI Lab (대규모 회로 및 시스템 연구실)

http://vlsi.snu.ac.kr

Principal Investigator

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Education:

1999 – 2004 Ph.D., Electrical and Computer Engineering, Purdue University, USA
1996 – 1998 M.S., Electrical Engineering, Seoul National University, Korea
1990 – 1994 B.S., Electronics Engineering, Seoul National University, Korea

Experiences:

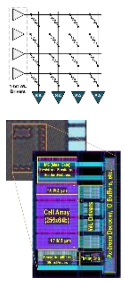
2021.9 – Present, Professor, Electrical and Computer Engineering, Seoul National University
2019.3 – 2021.8, Professor, Convergence IT Engineering, POSTECH
2013.2 - 2019.2, Associate Professor, Convergence IT Engineering, POSTECH
2004.5 – 2013.1, Research Staff Member, IBM T. J. Watson Research Center, USA

Research Area

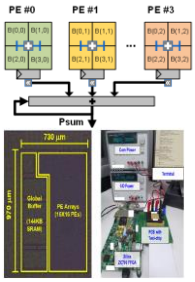
Neural Processing Unit (NPU) Design

We design energy-efficient and high-performance deep learning hardware accelerators.

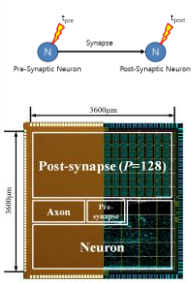
Our achievements include
- In-memory neural network algorithm/hardware design
- Variable-precision neural network chip
- Area-efficient spiking neural network (SNN) chip



SRAM In-memory BNN chip



Variable-precision NPU

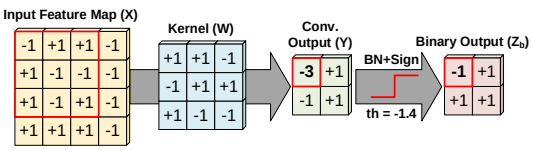


SNN Chip

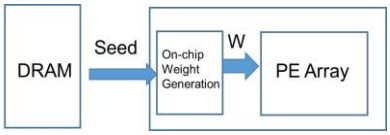
On-device AI: Neural network compression

We make the neural network lighter to enable deep learning computation in energy-constrained embedded computing devices.

Our achievements include
- High-accuracy binary neural networks (BNN)
- Sub-4b neural network quantization
- Viterbi-coding based pruning algorithms



Binary Neural Network (1b weight/activation)

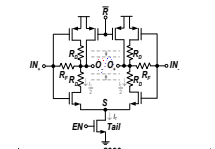


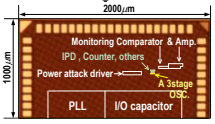
Viterbi-based Neural Network Pruning

Low-Power VLSI Design

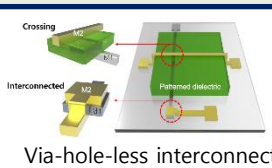
We invent various circuits with low-power and variation-aware characteristics.

Our achievements include
- CMOS true-random number generator chip
- On-chip timing error detection / correction circuits for flip-flop based pipeline
- Device/circuit co-design

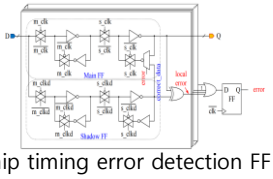




CMOS TRNG chip



Via-hole-less interconnect



On-chip timing error detection FF